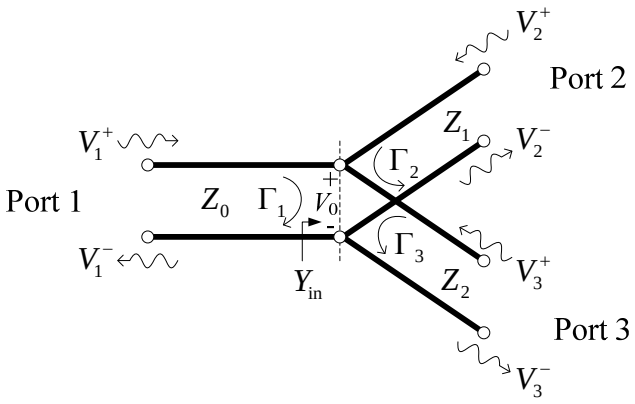
Lecture 24: T-Junction and Resistive Power Dividers.

The first class of three-port networks we'll consider is the T-junction power divider. We will look at lossless, nearly lossless, and lossy dividers in this and the next lecture.

A simple lossless T-junction network is shown in Fig. 7.6:



(Fig. 1)

There are two basic constraints we need to incorporate into this power splitter:

1. The feedline should be matched.
2. The input time average power, P_{in}, should be divided between ports 2 and 3 in a desired ratio.

   In the text, this ratio is defined as $X{:}Y$ where:

   - $X/(X+Y)\cdot 100\%$ of the incident power is delivered to one output port, and
   - $Y/(X+Y)\cdot 100\%$ of the incident power is delivered to the other.

For example:

- 1:1 means 50% of the incident time average power is delivered to each output port.
- 2:1 means 67% of the incident time average power is delivered to one output port and the remaining to the other.

Referring to the circuit above, in order to enforce the first constraint on the power splitter requires that

$$Y_{\text{in}} = \frac{1}{Z_1} + \frac{1}{Z_2} = \frac{1}{Z_0} \qquad (7.25),(1)$$

Consequently, to divide the incident power between the two output ports, we simply need to adjust the characteristic impedances of the two TLs.

Because port 1 is matched, the input time average power is simply:

$$P_{\text{in}} = \frac{1}{2}\frac{\left|V_1^+\right|^2}{Z_0} = \frac{1}{2}\frac{\left|V_0\right|^2}{Z_0} \qquad (2)$$

where V_0 is the phasor (total) voltage at the junction.

The output powers can be computed similarly, since we assume both of the ports are matched, as

$$P_1 = \frac{1}{2}\frac{\left|V_0\right|^2}{Z_1} \quad \text{and} \quad P_2 = \frac{1}{2}\frac{\left|V_0\right|^2}{Z_2} \qquad (3),(4)$$

Dividing (3) and (4) by (2) we find

$$\frac{P_1}{P_{\text{in}}} = \frac{1/Z_1}{1/Z_0} = \frac{Z_0}{Z_1} \quad \text{and} \quad \frac{P_2}{P_{\text{in}}} = \frac{1/Z_2}{1/Z_0} = \frac{Z_0}{Z_2} \qquad (5),(6)$$

Because the network is lossless:

$$\frac{P_1}{P_{\text{in}}} + \frac{P_2}{P_{\text{in}}} = 1$$

Substituting (5) and (6) into this expression gives

$$\frac{Z_0}{Z_1} + \frac{Z_0}{Z_2} = 1 \quad \text{so that} \quad \frac{1}{Z_1} + \frac{1}{Z_2} = \frac{1}{Z_0}$$

Consequently, not only have we split the power between the output ports, but in light of (1) we have also ensured that the feedline is matched.

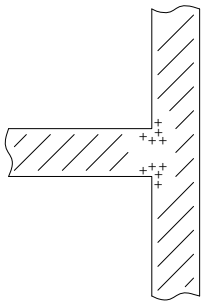
So, once we have specified the desired ratios for the output port powers, we can use (5) and (6) to compute the required characteristic impedances of these TLs:

$$\boxed{Z_1 = \frac{Z_0}{P_1/P_{\text{in}}}} \quad \text{and} \quad \boxed{Z_2 = \frac{Z_0}{P_2/P_{\text{in}}}} \qquad (7),(8)$$

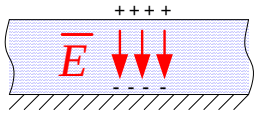
That's basically it for the design of a simple T-junction power divider. An example of this design process is given in Example 7.1 of the text, which we'll cover later.

From a practical standpoint, there are two important points that arise with T-junction power splitters:

1. Junction effects. At the junction of the TLs, there is likely to be an accumulation of excess charge. Take a microstrip junction for example:



These charges attract oppositely-signed charges on the ground plane:

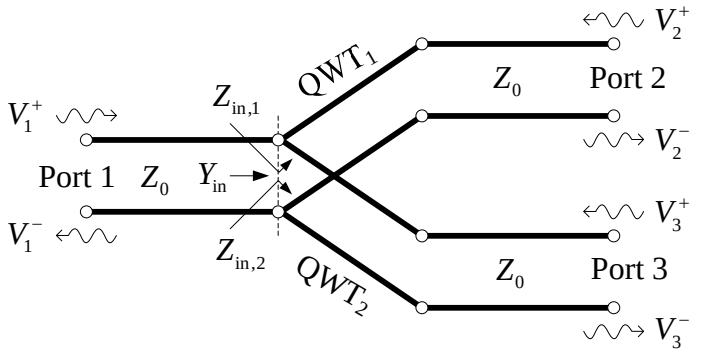


This time-varying electric field is a displacement current, of course. We can model this effect as a lumped capacitor connected to ground, as shown in Fig. 7.6.

2. Characteristic impedance of the output lines. It is not too practical to have these Z_1 and Z_2 characteristic impedances in the system. We generally like to work with just one system impedance, Z_0.

One approach to resolve this issue would be to add impedance matching circuits to the ends of the ports 2 and 3 in Fig. 1. (Some of your homework problems may specify that you do that.) Here, however, we'll do something

different. We'll use QWT's as impedance transforming devices:



The QWT's act to transform Z_0 to $Z_{in,1}$ and Z_0 to $Z_{in,2}$. Using QWTs makes this power splitter more narrow-banded, unfortunately.

Here, instead of Z_1 and Z_2 in the design equations (7) and (8), the impedances of interest in the power splitter design are $Z_{in,1}$ and $Z_{in,2}$. From (1), the match condition now becomes

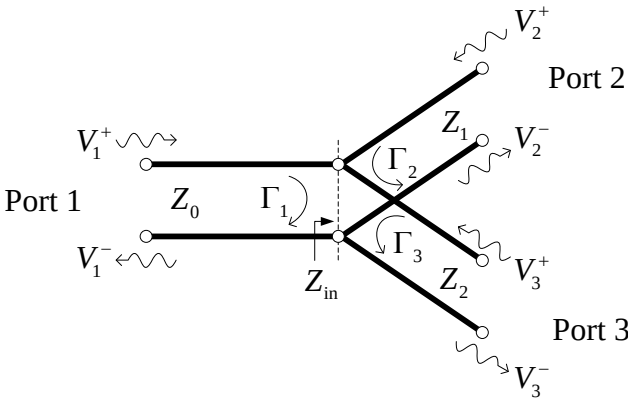
$$\frac{1}{Z_{in,1}} + \frac{1}{Z_{in,2}} = \frac{1}{Z_0} \qquad (9)$$

and from (5) and (6), the power division constraints become

$$\boxed{\frac{P_1}{P_{in}} = \frac{Z_0}{Z_{in,1}}} \quad \text{and} \quad \boxed{\frac{P_2}{P_{in}} = \frac{Z_0}{Z_{in,2}}} \qquad (10),(11)$$

Example N24.1 (based on text example 7.1). Design a 1:2, T-junction power divider in a 50-Ω system impedance.

We'll choose to use the network in Figure 7.6 with $B = 0$:



For a 1:2 split, we want line 1 to carry $P_{in}/3$ and line 2 to carry $2P_{in}/3$.

From (7) and (8):

$$Z_1 = \frac{50}{1/3} = 150\ \Omega \quad \text{and} \quad Z_2 = \frac{50}{2/3} = 75\ \Omega$$

That's it for the design of the splitter.

We'll carry this example further and first check to make sure the input port is matched. For a lossless network, $P_1/P_{in} + P_2/P_{in} = 1$ which implies that $1/Z_1 + 1/Z_2 = 1/Z_0$. In this example,

$$\frac{1}{150} + \frac{1}{75} = \frac{1}{50}$$

Therefore, $Z_{in} = 50\ \Omega$ as needed and as expected.

Second, we'll compute the *S* parameters for this network. We know that $S_{11} = 0$ since we just computed $Z_{in} = 50\ \Omega$.

The network is reciprocal, so $[S]$ must be symmetrical. The network is also lossless and because it's a three-port, we know that not all ports will be simultaneously matched. That is, port 2 (port 3) will not be matched when ports 1 and 3 (ports 1 and 2) are terminated with matched loads.

Based on these facts, we can surmise that the *S* matrix will have the form:

$$[S]=\begin{bmatrix} 0 & S_{21} & S_{31} \\ S_{21} & S_{22} & S_{32} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \tag{12}$$

Let's now compute these *S* parameters:

- **S_{22}.** Terminating port 1 with 50 Ω and port 3 with 75 Ω, we find

$$S_{22}=\Gamma_2\big|_{V_1^+=V_3^+=0}=\frac{Z_0\,||\,Z_2-Z_1}{Z_0\,||\,Z_2+Z_1}=-\frac{2}{3}$$

- **S_{33}.** Terminating port 1 with 50 Ω and port 2 with 150 Ω, we find

$$S_{33}=\Gamma_3\big|_{V_1^+=V_2^+=0}=\frac{Z_0\,||\,Z_1-Z_2}{Z_0\,||\,Z_1+Z_2}=-\frac{1}{3}$$

- **S_{21}=S_{12}.** Terminating port 2 with 150 Ω and port 3 with 75 Ω, then

$$V_1^+\left(1+\Gamma_1\right)=V_2^-$$

therefore $$\left.\frac{V_2^-}{V_1^+}\right|_{V_2^+=V_3^+=0} = 1+\Gamma_1 \underbrace{=}_{\Gamma_1=0} 1$$

One subtlety here is the port 1 and port 2 impedances are different. Consequently, we need to use generalized *S* parameters. From Lecture 17:

$$S_{ij} = \left.\frac{V_i^- \sqrt{Z_{0,j}}}{V_j^+ \sqrt{Z_{0,i}}}\right|_{V_k^+=0,\ \forall k\neq j} \qquad (4.62)$$

so that here

$$S_{21} = \left.\frac{V_2^- \sqrt{Z_{0,1}}}{V_1^+ \sqrt{Z_{0,2}}}\right|_{V_2^+=V_3^+=0} = 1\cdot\frac{\sqrt{50}}{\sqrt{150}} = 0.577$$

- **$S_{31}=S_{13}$.** Terminating port 2 with 150 Ω and port 3 with 75 Ω, then

$$V_1^+\left(1+\Gamma_1\right) = V_3^-$$

so that $$\left.\frac{V_3^-}{V_1^+}\right|_{V_2^+=V_3^+=0} = 1+\Gamma_1 \underbrace{=}_{\Gamma_1=0} 1$$

Hence, $$S_{31} = \left.\frac{V_3^- \sqrt{Z_{0,1}}}{V_1^+ \sqrt{Z_{0,3}}}\right|_{V_2^+=V_3^+=0} = 1\cdot\frac{\sqrt{50}}{\sqrt{75}} = 0.816$$

- **$S_{32}=S_{23}$.** Terminating port 1 with 50 Ω and port 3 with 75 Ω, then

$$V_2^+\left(1+\underbrace{\Gamma_2}_{=-2/3}\right)=V_3^-$$

so that $$S_{32}=\left.\frac{V_3^-\sqrt{Z_{0,2}}}{V_2^+\sqrt{Z_{0,3}}}\right|_{V_1^+=V_3^+=0}=\left(1-\frac{2}{3}\right)\cdot\frac{\sqrt{150}}{\sqrt{75}}=0.471$$

This relatively large value of S_{32} indicates there is little isolation between the two output ports. This is often undesirable.

Since the network is lossless, implying that $[S]$ is unitary, then from (12):

$$|S_{11}|^2+|S_{21}|^2+|S_{31}|^2=1$$

or

$$|S_{21}|^2+|S_{31}|^2=1$$

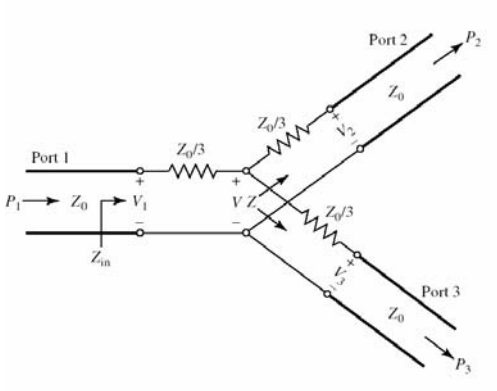
Substituting for S_{21} and S_{31}, we find that

$$|S_{21}|^2+|S_{31}|^2=0.333+0.666=0.999$$

which serves to partially verify the correctness of our S parameter calculations.

Resistive Divider Power Splitter

This type of divider is shown in Figure 7.7 and is constructed from three resistors:



Since this network is lossy, the resistive power divider can be simultaneously matched at all three ports. However, the two output ports will most likely not be isolated.

The *S*-parameter analysis of this three-port can be performed using only simple circuit theory since all three ports will be matched. With no reflections from the port, the total port voltages are simply the amplitudes of the incoming or outgoing voltage waves, as appropriate for that port.