Lecture 31: JFETs as Variable Resistors

One nice feature of the NorCal 40A is the Automatic Gain Control (AGC). This circuit keeps the audio output at a reasonably constant level as you tune across the band and receive very strong or weak signals.

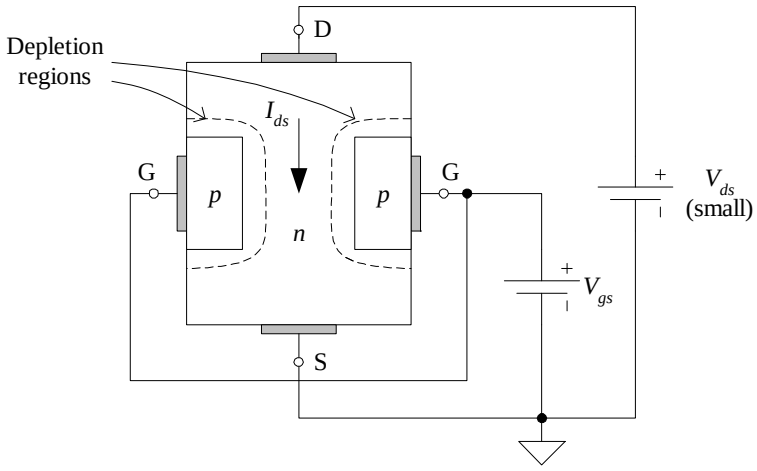
A key part of the AGC is the pair of JFETs Q2 and Q3. These are simply J309s, as we used for the Buffer Amplifier (Q5) and the VFO (Q8).

As we'll see, Q2 and Q3 in the AGC simply act as voltage controlled variable resistors! For the remainder of this lecture, we will discuss this valuable behavior of JFETs, while in the next lecture we will discuss the details behind the AGC.

JFET with an Open Channel (Triode Region)

Recall from our previous discussion on JFETs in Lecture 21 that an *n*-type JFET can be physically approximated by the geometry shown in the figure below.

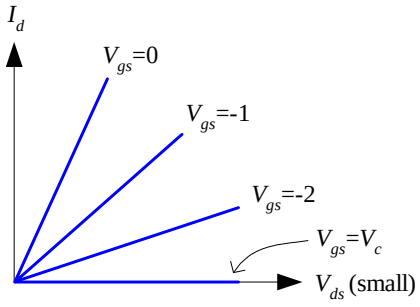
The JFET has a negative V_{gs} which increases the depletion regions (and decreases the channel width) as V_{gs} is made more negative.



Current I_{ds} will flow from drain to source. The amount of current (at a given V_{ds}) depends on the channel resistance, r_{ds}.

As V_{gs} becomes more negative, the depletion regions grow wider and the channel narrows. Consequently, the channel resistance r_{ds} increases.

Assuming V_{ds} is small enough, this behavior can be represented by straight lines of varying slope in a characteristic plot of the JFET transistor:



As V_{gs} becomes more negative, eventually the two depletion regions combine and the channel is depleted of all charge carriers (e^- for n channel) and no current will flow. This

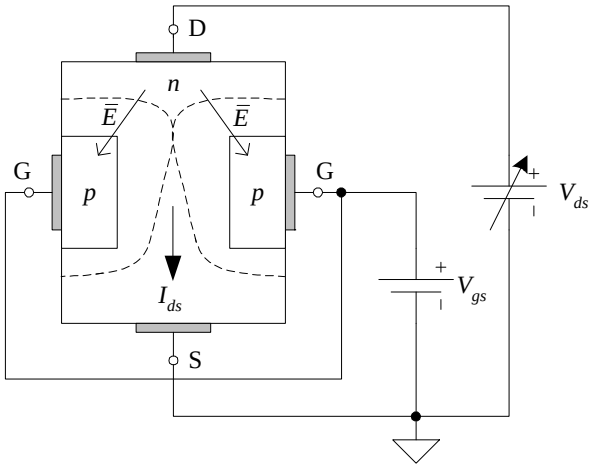
particular V_{gs} is the JFET pinch off (or cut off) voltage V_c. It is a negative number for *n*-channel JFETs.

We can view this effect in a JFET as a voltage controlled resistance (VCR).

Saturated JFETs

For completeness, we'll quickly mention what happens to the channel as V_{ds} becomes large, though this is not the regime in which Q2 and Q3 operate in the NorCal 40A.

As V_{ds} increases, V_{gs} remains constant while the reverse bias "voltage" of each *pn* junction will increase as we move up the channel. This will give a tapered shape to the depletion region:



The channel becomes pinched off at the **drain** end when

$$V_{gd} = V_c$$

However, current still flows in the channel because charge carriers can drift through this relatively small depletion region.

Note that this "pinch off" is not the same as the JFET being completely pinched off so that no current can flow. Here, pinch off is occurring only at the drain end of the device.

Also, notice that as V_{ds} increases from this pinched off state, there will be little change in I_d! The maximum I_d occurs when $V_{gs} = 0$ and is defined as I_{dss}, the drain-to-source current with the gate shorted. There is maximum I_d in this case because with $V_{gs} = 0$, the channel is depleted only near the drain end.

As V_{gs} (< 0) varies, a larger region of the channel becomes depleted. This implies r_{ds} increases, which implies a smaller I_d. From this behavior, we can generate a family of characteristic curves as shown in Fig. 13.4:

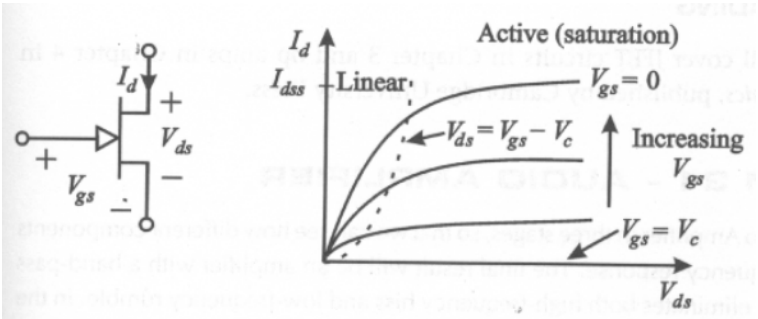


Figure 13.4. Drain current characteristics for a JFET.

When the JFET is biased with a "large" V_{ds} and $V_c < V_{gs} < 0$, it will operate in the so-called active (or saturation) region.

Linear or Triode Region of the JFET

In the Automatic Gain Control (AGC) circuit of the NorCal 40A, the JFETs Q2 and Q3 are operated not in the active (i.e., the saturation) region. Rather, they are operated in the JFET linear region (also called the triode region or VCR region). In this linear region shown above in Fig. 13.4, the drain current is expressed as

$$I_d = V_{ds}\left(\frac{2I_{dss}}{V_c^2}\right)\left(V_{gs} - V_c - \frac{V_{ds}}{2}\right) \text{ [A]} \qquad (13.12)$$

For small V_{ds} [$\ll 2\left(V_{gs} - V_c\right)$], as is the case in the linear region,

$$I_d \approx V_{ds}\left(\frac{2I_{dss}}{V_c^2}\right)\left(V_{gs} - V_c\right) \text{ [A]} \qquad (1)$$

By definition, the channel resistance r_{ds} is computed as

$$r_{ds} = \left.\frac{V_{ds}}{I_d}\right|_{V_{ds}\ \text{small}} \text{ [}\Omega\text{]} \qquad (2)$$

Using (1) in (2) we find for small V_{ds} that

$$r_{ds} \approx \left[2\frac{I_{dss}}{V_c^2}\left(V_{gs} - V_c\right)\right]^{-1} \underset{(13.13)}{\equiv} \frac{1}{G} \text{ [}\Omega\text{]} \qquad (3)$$

Plots of these two quantities in (3) are shown in Fig. 13.5:

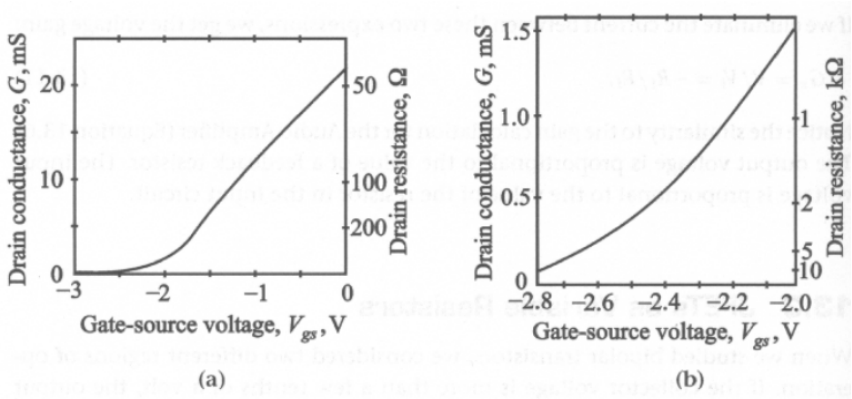


Figure 13.5. Drain conductance in the linear region for the J309 JFET as a function of the gate voltage (a), and the high-resistance region near cutoff (b).

JFETs in the AGC

So how are the JFETs applied as variable controlled resistors in the NorCal 40A? Fig. 13.9 shows them as the AGC attenuators:

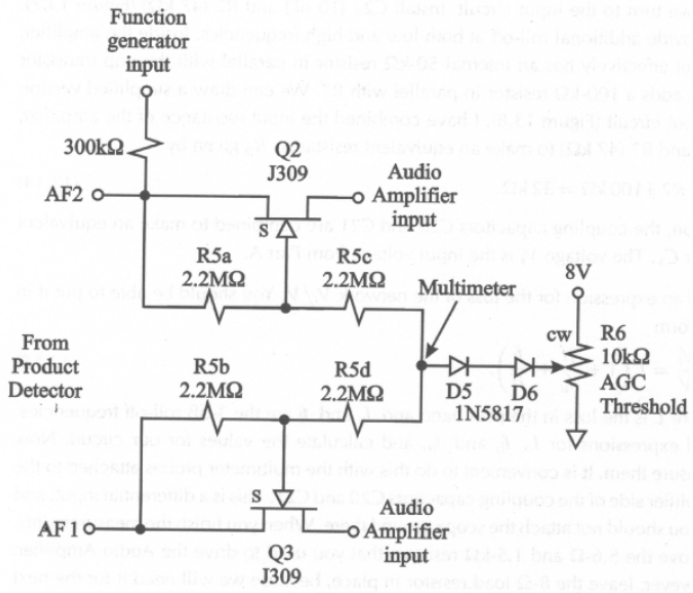
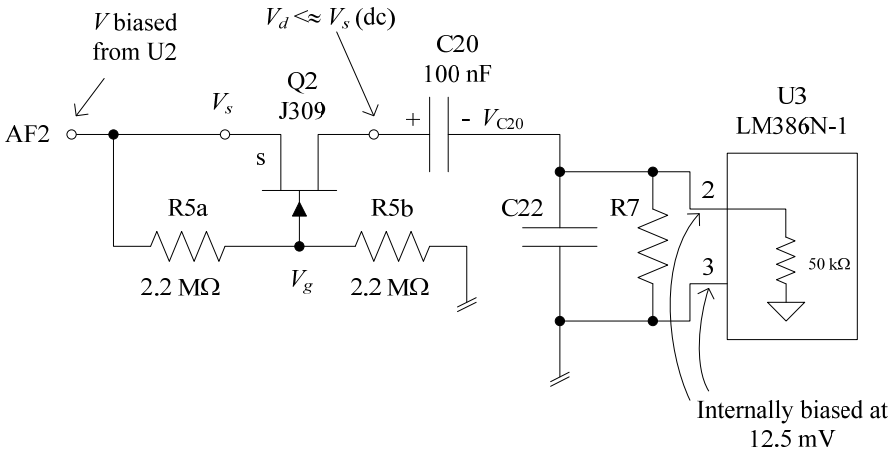


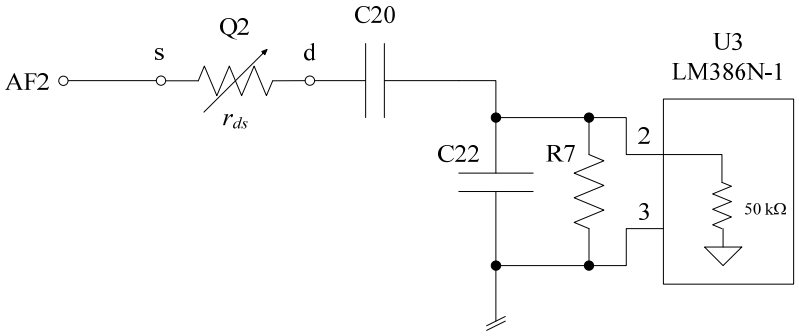
Figure 13.9. The AGC attenuators.

More specifically, consider the Q2 circuit connected to U3:



C20 charges to $V_{C20} \lessapprox V_s$ through Q2 and the internal 50-kΩ resistor at pin 2 of U3. V_d will be slightly less than V_s because of the Q2 channel resistance. Because of this, $|V_{ds}|$ is small, which implies Q2 operates in the triode region. The VCR control voltage is V_{gs}.

Here is an equivalent model for this Q2 circuit:



A similar model applies to the Q3 circuit.

We'll see in the next lecture that the AGC will vary r_{ds} in response to the output voltage at the speaker.