Lecture 21: Junction Field Effect Transistors. Source Follower Amplifier

As mentioned in Lecture 16, there are two major families of transistors. We've worked with BJTs in the past few lectures.

The second transistor type we will consider is the field effect transistor (FET). In the NorCal 40A, we use discrete junction field effect transistors (JFETs). (Recall that in ICs, metal oxide semiconductor FETs are usually used.)

Four important points concerning the JFET are:

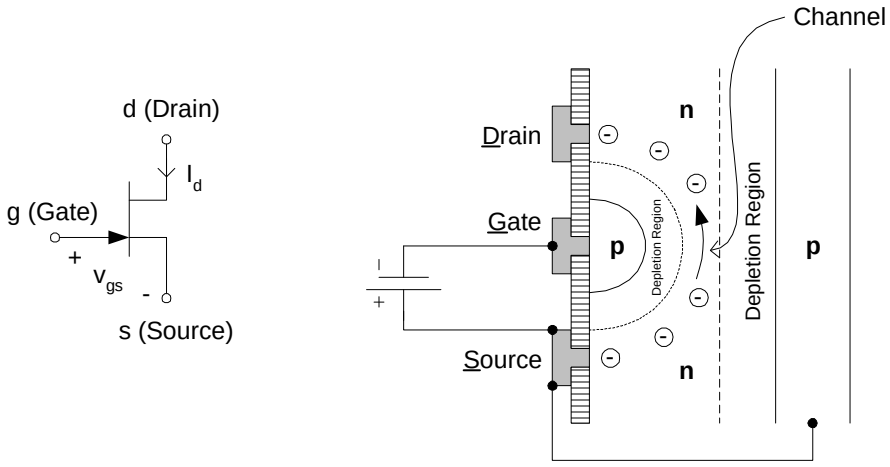
1. Probably the simplest transistor,
2. Very large input impedance (but MOSFETs even larger),
3. Virtually obsolete compared to the MOSFET,
4. Now used mainly in discrete circuit design – switches, amplifiers, etc.

In the NorCal 40A, JFETs are used in the:

1. Buffer Amplifier (as a buffer amplifier–duh!),
2. Variable Frequency Oscillator, VFO (as the gain element in the oscillator),
3. Automatic Gain Control, AGC (as a voltage controlled variable resistance).

Physical Behavior of Junction Field Effect Transistors

As with BJTs, there are *n* and *p* type JFETs. We use only *n*-type in the Norcal 40A (the J309).



Notice that the gate is reversed biased wrt the source, which is itself often connected to the *p*-type body.

By making V_{gs} more negative, the gate *pn* junction develops a larger depletion region. This has the effect of narrowing the channel and, consequently, decreasing I_d (the drain current).

Eventually, when

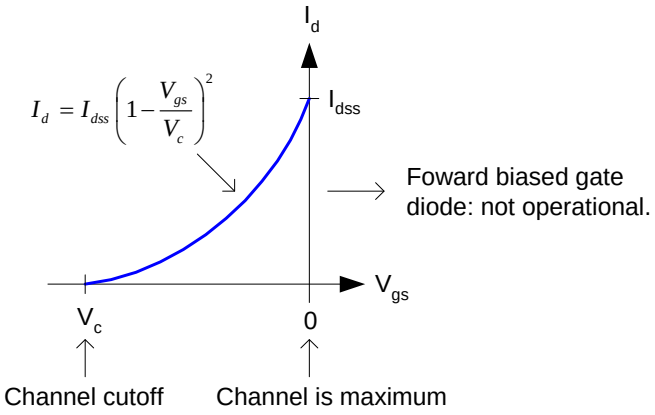
$$V_{gs} = V_c \left(< 0\right)$$

the channel becomes closed (or "pinched off"). V_c is called the cutoff voltage and is less than zero. (For the J309, $V_c \approx -2.5$ V.)

Mathematically, the drain current is expressed as

$$I_d = I_{dss}\left(1-\frac{V_{gs}}{V_c}\right)^2 \quad [\text{A}] \tag{9.74}$$

I_{dss} is the drain to source current with the gated shorted to the source. This characteristic curve is shown in Fig. 9.15:



The slope of this drain current versus V_{gs} is called the transconductance g_m of the JFET:

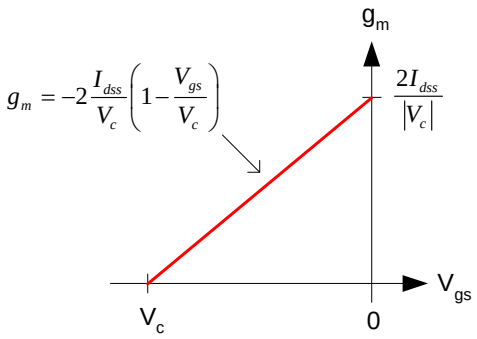
$$g_m = \frac{dI_d}{dV_{gs}} \quad [\text{S}] \tag{9.75}$$

The significance of g_m to a JFET is analogous to β for a BJT.

Substituting (9.74) into (9.75) and performing the differentiation gives

$$g_m = -2\frac{I_{dss}}{V_c}\left(1-\frac{V_{gs}}{V_c}\right) \quad [\text{S}] \tag{9.76}$$

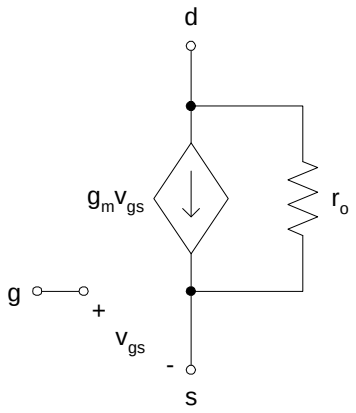
This curve is simply a straight line, as shown in Fig 9.16:



Interestingly, we see that g_m actually *changes* as V_{gs} changes. The β for BJTs did not have such dependence. Later in Section 11.4 (and Probs. 26 and 27), we will harness this behavior of JFETs to make a nice oscillator!

Small Signal Model of the JFET

The low frequency, small signal model for an *n*-type JFET is shown in Fig. 9.17a:



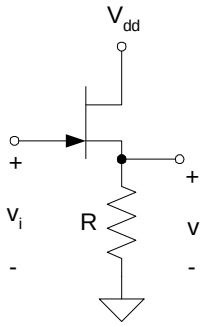
The gate is open circuited, which models the extremely large input impedance of properly biased JFETs (remember that the

input can be a reversed-biased *pn* junction). This input impedance is easily greater than 1 MΩ.

In the model above, r_o is the output resistance of the JFET. It's often neglected in paper analysis of these circuits. (However, in Prob. 27, $r_d = r_o = 5$ kΩ is used in second-order calculations.)

Source Follower FET Amplifier

A JFET source follower amplifier is very similar to the BJT emitter follower (Fig. 9.17b):



The FET source follower (1) has a very large input impedance, (2) is very simple to bias, and (3) has $G_v \lessapprox 1$.

The source follower is used in the Buffer Amplifier (Q5) in the NorCal 40A. The Buffer Amplifier isolates the Transmit Filter from the Driver Amplifier. This isolation keeps changes in the input impedance to the Driver Amplifier from affecting the Transmit Filter. [See (9.36) in your text.]

Surprisingly, *R* alone is **all** that's needed to set the bias of the source follower, provided the gate is dc grounded (but, of course, not ac grounded!).

As an example of a dc grounded gate, consider the Buffer Amplifier in the NorCal 40A. Notice that R10 and L6 provide a dc path to ground so there is no dc current. Also, notice that ac signals at the gate are *not* grounded.

The dc source voltage in the above circuit is

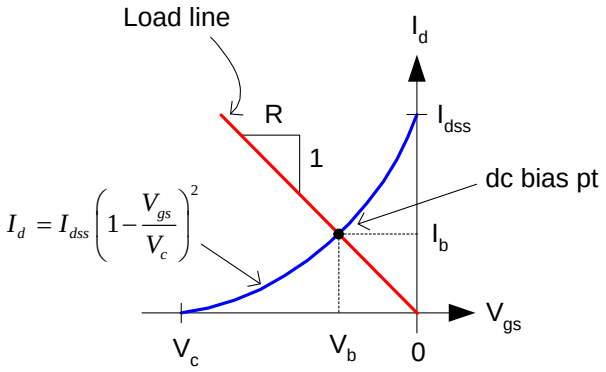
$$V_s = I_b R$$

where I_b is the drain to source bias current. Then,

$$V_{gs} = V_g - V_s = 0 - I_b R = -I_b R \qquad (9.77)$$

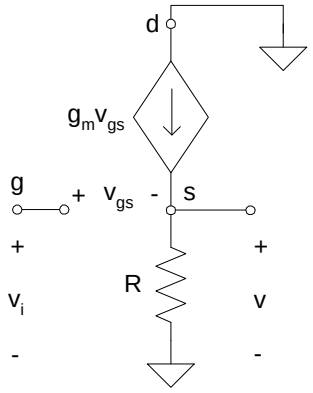
This is simply an equation for a straight line. This straight line is the load line and we can use it together with the JFET characteristic equation (9.74) to determine the dc bias point for V_{gs} and I_{ds}.

Referring to Fig. 9.18:



The intersection of the load line with the JFET characteristic curve gives a graphical solution for the dc bias point of the source follower amplifier: $V_{gs} = V_b$ and $I_d = I_b$.

Once the source follower has been properly biased, the ac output impedance and the voltage gain can be easily determined. The small-signal equivalent circuit model for the source follower amplifier is (Fig. 9.17c):



From this circuit we see that

$$v = g_m v_{gs} R \tag{9.78}$$

where

$$v_{gs} = v_g - v_s = v_i - v \tag{9.79}$$

Substituting (9.79) into (9.78) we find

$$v = g_m R\left(v_i - v\right) = g_m R v_i - g_m R v$$

or

$$\left(1 + g_m R\right) v = g_m R v_i$$

Now solving for the ratio of output to input voltage we find

$$\frac{v}{v_i} \equiv G_v = \frac{g_m R}{1 + g_m R}$$

or $$G_v = \frac{1}{1+\frac{1}{g_m R}} \tag{9.82}$$

where G_v is the small signal voltage gain.

The JFET transconductance is usually quite small. But if we choose R such that $g_m R \gg 1$ (i.e., $R \gg g_m^{-1}$), then

$$G_v \lessapprox 1$$

which is typical for a source-follower JFET amplifier.