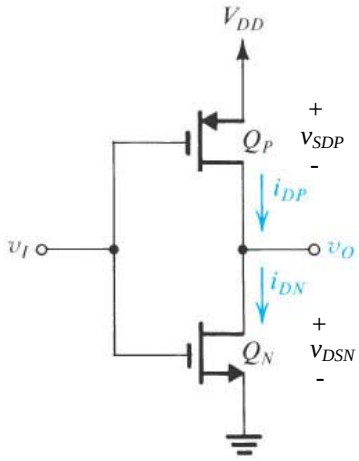
Lecture 37: CMOS Digital Logic Inverter.

The basic circuit element for digital circuit design is the logic inverter. This element is used to build logic gates and more complicated digital circuits.

The basic CMOS logic inverter is shown in Fig. 14.22. We'll assume the body and source terminals are connected together, so there's no body effect to consider. We'll also assume that the MOSFETs are matched transistors.

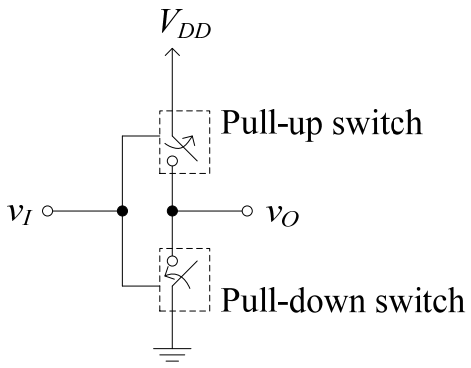


(Fig. 14.22)

The operation of this circuit can be summarized as:

- When v_I is "low," Q_N is "off," Q_P is "on" $\Rightarrow$ v_O is "high"
- When v_I is "high," Q_N is "on," Q_P is "off" $\Rightarrow$ v_O is "low"

Conceptually, this CMOS circuit is intended to function as "complementary switches" shown in Fig. 14.18(a):



(Fig. 14.18a)

The directions of the arrows indicate the complementary nature of the two switches: when one is closed the other is open, and *vice versa*.

Graphical Analysis of the CMOS Logic Inverter

A more complete analysis of this CMOS logic inverter can be performed graphically, as shown in Figs. 14.23 and 14.24. Here, Q_P is treated as an active load for Q_N, though the converse would produce identical results. We'll consider the two extremes of the input: $v_I = 0$ ("low") and $v_I = V_{DD}$ ("high").

With Q_N considered the driving transistor and Q_P the active load, then for a graphical solution we'll be plotting characteristic and load curves in the i_{DN}-v_{DSN} plane.

For this digital logic inverter circuit in Fig. 14.22, we see that $i_{DP} = i_{DN}$.

The v_{DS} values are different for the two transistors, of course. By KVL,

$$V_{DD} - v_{SDP} = v_{DSN} \tag{1}$$

How we interpret this equation can give us the answers on how to plot the Q_P characteristic curve in the i_{DN}-v_{DSN} plane:

- The minus sign in (1) tells us to flip the Q_P characteristic curve about the vertical axis ($i_{DN} = i_{DP}$).
- The V_{DD} term tells us to shift this flipped curve V_{DD} units to the right.

(This is the same process we used for the graphical solution of the CMOS common source amplifier discussed in Lecture 33.)

Graphical solution when v_I is "high":

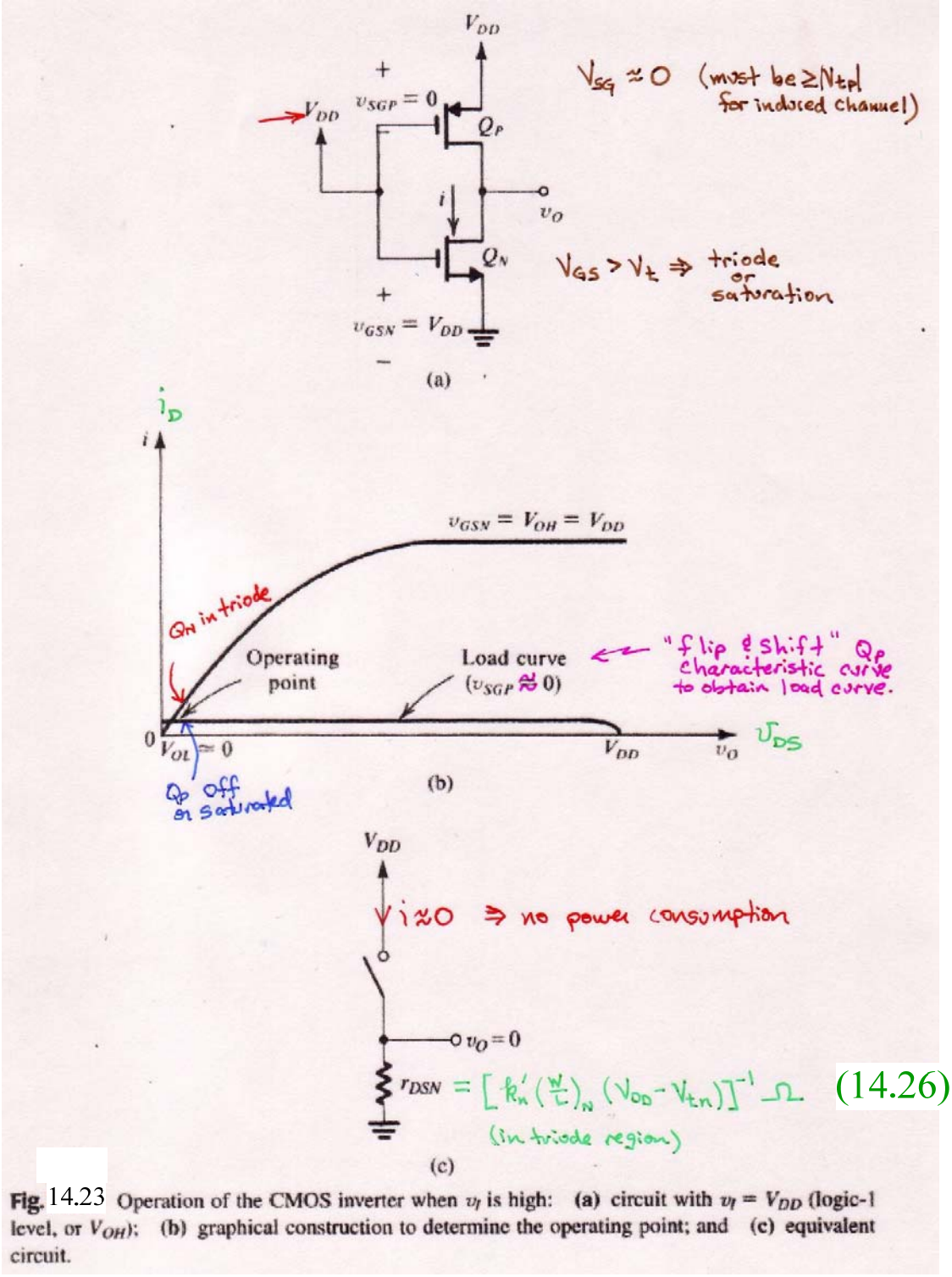


Fig. 14.23 Operation of the CMOS inverter when v_I is high: **(a)** circuit with $v_I = V_{DD}$ (logic-1 level, or V_{OH}); **(b)** graphical construction to determine the operating point; and **(c)** equivalent circuit.

Graphical solution when v_I is "low":

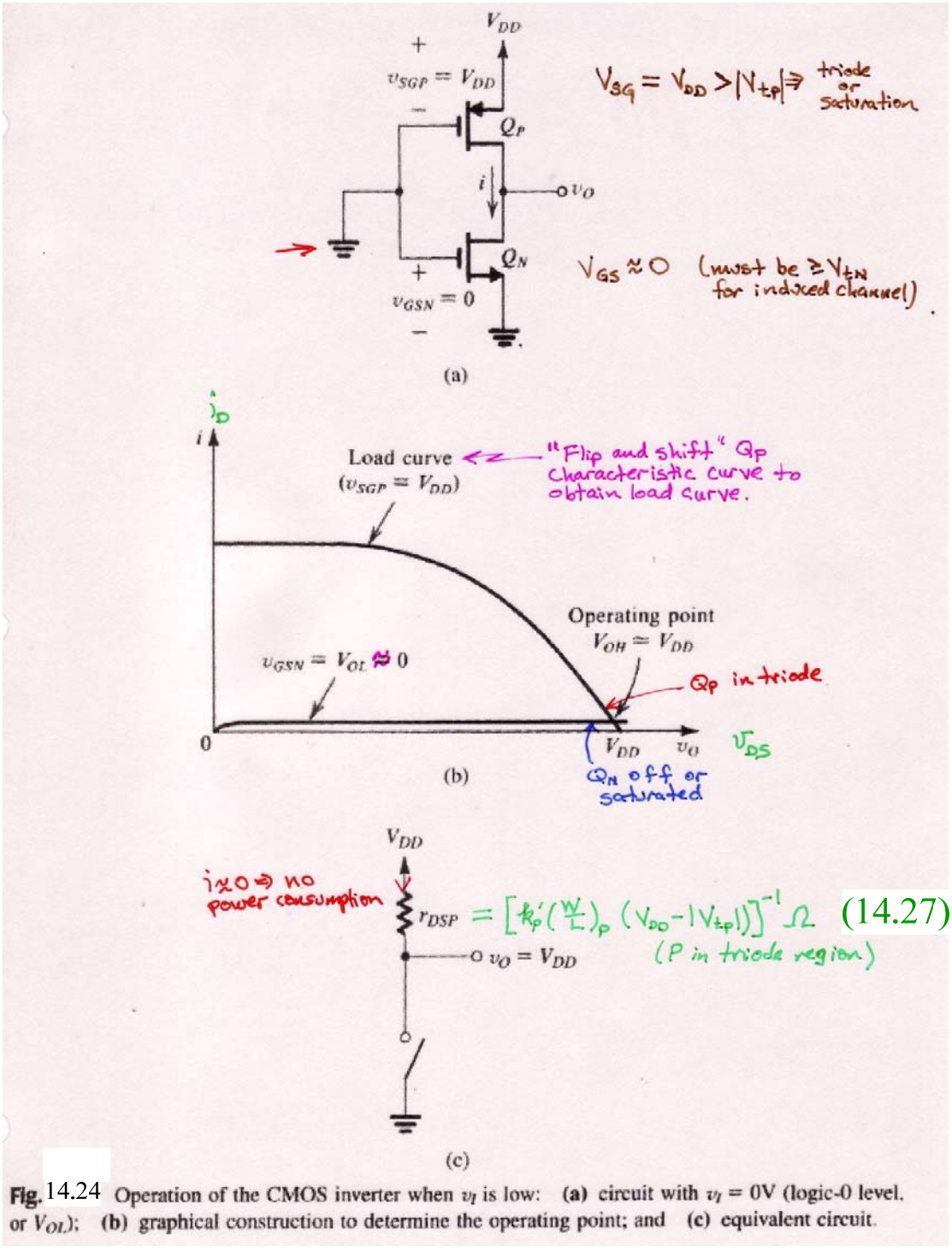


Fig. 14.24 Operation of the CMOS inverter when v_I is low: **(a)** circuit with v_I = 0V (logic-0 level, or V_{OL}); **(b)** graphical construction to determine the operating point; and **(c)** equivalent circuit.

Summary of the CMOS Digital Logic Inverter

1. The output voltage levels are ~10 mV and ~V_{DD}-10mV, thus the output signal swing is nearly the maximum possible. (Gives rise to the so-called noise margins.)

2. The static power dissipation is nearly zero (a fraction of a μW) in both states. The dynamic power dissipation is not zero as the gates are changing states.

3. Low output resistance in either state: low resistance to ground in the "low" output state, and low resistance to V_{DD} in the "high" state.

4. Input resistance of the inverter is very large (ideally infinite). The inverter can drive a very large number of similar inverters with little loss in signal level.

5. The gate input capacitance is not negligible, so it will take time to "charge" up. Low output resistance helps to keep the time constant $\tau = R_{\text{out}} C_{\text{in}}$ small when driving similar inverters.

Characteristic Curve for the CMOS Logic Inverter

In addition to the graphical solution we just performed, it is also fairly straightforward to numerically construct the characteristic curve v_O versus v_I.

To obtain an equation to plot for the inverter characteristic curve, we will use the equations for the MOSFET current in the triode and saturation regions of operation.

The i_D-v_{DS} characteristic curve for Q_N is given by

$$i_{DN} = k_n' \left(\frac{W}{L}\right)_n \left[\left(\underbrace{v_I}_{v_{GS}} - V_{tn}\right)\underbrace{v_O}_{v_{DS}} - \frac{1}{2}\underbrace{v_O^2}_{v_{DS}^2}\right] \qquad \underbrace{v_O}_{v_{DS}} \le \underbrace{v_I}_{v_{GS}} - V_{tn} \qquad (14.28),(2)$$

$$i_{DN} = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_n \left(\underbrace{v_I}_{v_{GS}} - V_{tn}\right)^2 \qquad \underbrace{v_O}_{v_{DS}} \ge \underbrace{v_I}_{v_{GS}} - V_{tn} \qquad (14.29),(3)$$

while the i_D-v_{DS} characteristic curve for Q_P is given by

$$i_{DP} = k_p' \left(\frac{W}{L}\right)_p \left[\left(\underbrace{V_{DD} - v_I}_{v_{GS}} - |V_{tp}|\right)\underbrace{(V_{DD} - v_O)}_{v_{SD}} - \frac{1}{2}\left(\underbrace{V_{DD} - v_O}_{v_{SD}}\right)^2\right] \qquad v_O \ge v_I + |V_{tp}| \qquad (14.30),(4)$$

$$i_{DP} = \frac{1}{2} k_p' \left(\frac{W}{L}\right)_p \left(\underbrace{V_{DD} - v_I}_{v_{GS}} - |V_{tp}|\right)^2 \qquad v_O \le v_I + |V_{tp}| \qquad (14.31),(5)$$

For the digital logic inverter circuit, these two currents must be equal:

$$i_{DN} = i_{DP} \qquad (6)$$

To construct the complete characteristic curve for this logic inverter, we solve (6) for v_O using (2) through (5) as v_I varies from 0 to V_{DD}.

In the case of symmetrical MOSFETs in which $V_{tn} = |V_{tp}|$ and $k_n'(W/L)_n = k_p'(W/L)_p$, the voltage transfer characteristic (VTC) curve will also be symmetrical, as shown below in Fig. 14.25.

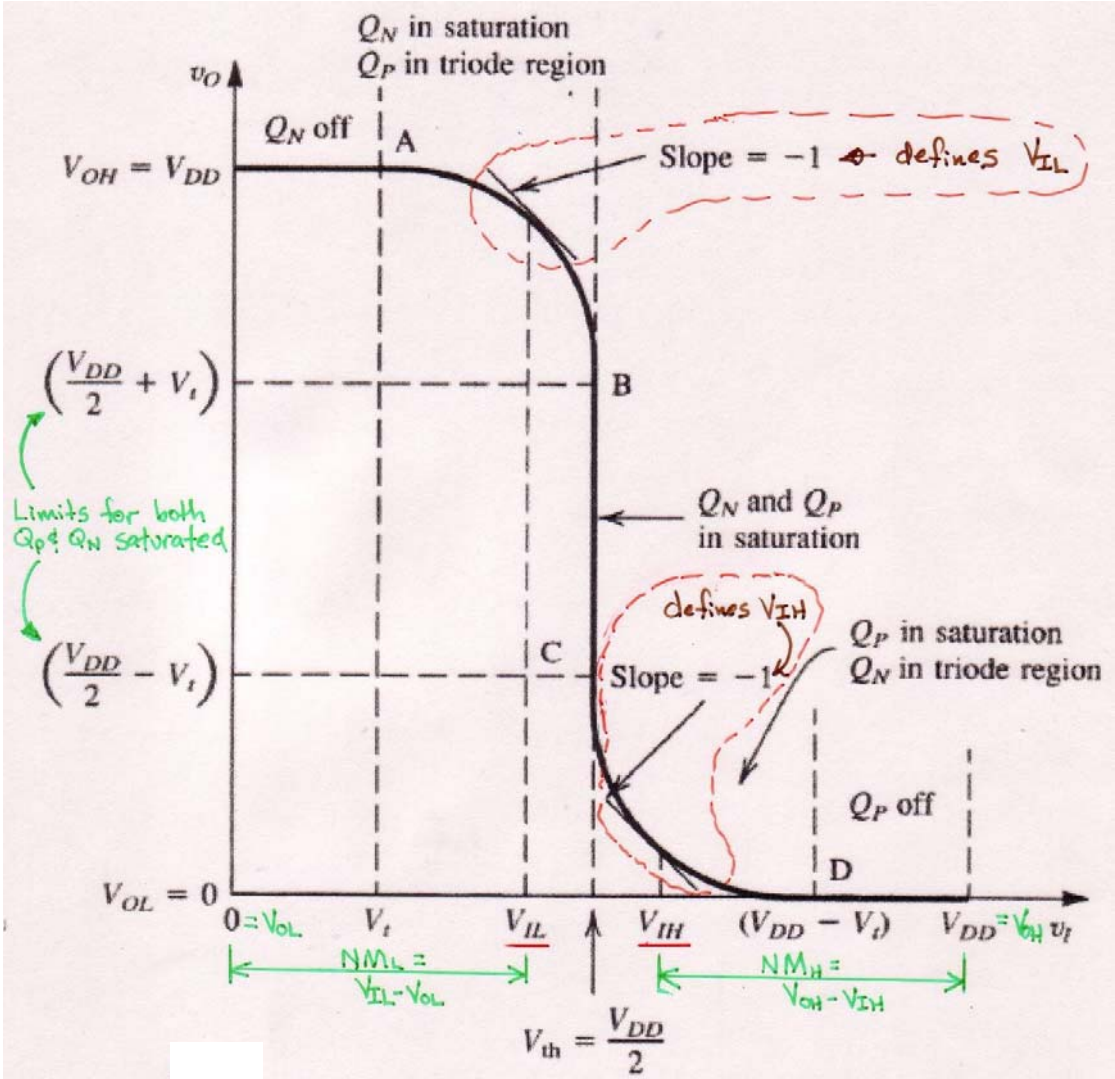


Fig. 14.25 The voltage transfer characteristic of the CMOS inverter.

$NM_H \equiv V_{OH} - V_{IH}$

As derived in text:

$NM_H = \frac{1}{8}(3V_{DD} + 2V_t)$ (14.37)

$NM_L = NM_H$ (14.38)

Note that the use of MOSFETs for a digital circuit such as this inverter in Fig. 14.25 is using the extremes of the VTC. This is very different than when MOSFETs are used as small signal amplifiers where the linear region of the VTC is used.

Noise Margins

We can observe from this characteristic curve that there is a range of input values (from 0 to V_{IL}) that produce a high output voltage, and a range of input values (from V_{IH} to V_{DD}) that produce a low output voltage. This is one important advantage that digital circuits have over analog ones.

These ranges of input voltages are called noise margins. In particular, the noise margin for high input NM_H is defined as:

$$NM_H \equiv V_{OH} - V_{IH} \qquad (14.9),(7)$$

and the noise margin for low input NM_L is defined as:

$$NM_L \equiv V_{IL} - V_{OL} \qquad (14.8),(8)$$

Referring to Fig. 14.25, the voltages V_{IH} and V_{IL} are defined where the slope of the characteristic curve is -1. Solving (6) at these two points, it's shown in the text that

$$V_{IH} = \frac{1}{8}\left(5V_{DD} - 2V_t\right) \qquad (14.35),(9)$$

and

$$V_{IL} = \frac{1}{8}\left(3V_{DD} + 2V_t\right) \qquad (14.36),(10)$$

Using (9) and (10) in (7) and (8) we can determine expressions for the two noise margins to be

$$NM_H = \frac{1}{8}\left(3V_{DD} + 2V_t\right) \qquad (14.37),(11)$$

and $$NM_L = NM_H = \frac{1}{8}\left(3V_{DD} + 2V_t\right)$$ (14.38),(12)

These two noise margins are equal because we assumed the two MOSFETs in the inverter circuit to be symmetrical.

[Add material on propagation delay? Section 14.4]