Lecture 30: Biasing MOSFET Amplifiers. MOSFET Current Mirrors.

There are two different environments in which MOSFET amplifiers are found, (1) discrete circuits and (2) integrated circuits (ICs). The methods of biasing transistor amplifiers are different in these two environments.

Why? Primarily because it’s “expensive” to fabricate resistors (and large capacitors) on ICs. Of course, this is not a problem for discrete component circuits.

We will discuss these two environments separately.

Biasing Discrete MOSFET Amplifier Circuits

The methods we can use here are virtually identical to the BJT amplifier circuits we saw in Chapter 5. A few of these biasing topologies are:

(Fig. 4.30d)
Example N30.1. Design the MOSFET amplifier below so that $I_D = 1$ mA and allow for a drain voltage swing of $\pm 2$ V. The amplifier is to present a 1-MΩ input resistance to a capacitively coupled input signal. The transistor has $k_n' W/L = 0.5$ mA/V² and $V_t = 2$ V.
We can see directly from this circuit that at DC, $V_G = 0$. Recall that for operation in the saturation mode $V_{GD} \leq V_t$ (with $V_{GS} > 0$).

Now, for $\pm 2$-V swing in $v_o$ and large AC gain, we want $R_D$ to be large. Hence, let’s choose $V_D = 0$ (since $V_t = 2$ V). Then for this $\pm 2$-V swing in $v_o$

$$V_{GD}\bigg|_{min} = 0 - 2 = -2 \text{ V} < V_t$$

and

$$V_{GD}\bigg|_{max} = 0 + 2 = 2 \text{ V} = V_t$$

Because of these results, the MOSFET stays in saturation.

Consequently, with $V_D = 0$

$$R_D = \frac{V_{DD} - V_D}{1 \text{ mA} \over 1 \text{ mA}} = \frac{10 - 0}{1 \text{ mA}} = 10 \text{ k}\Omega$$

For a saturated MOSFET

$$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2 = 0.25 \times 10^{-3} (V_{GS} - 2)^2$$

For $I_D = 1 \text{ mA} \Rightarrow (V_{GS} - 2)^2 = 4$

or

$$V_{GS} = \pm 2 + 2 = +4 \text{ V} \text{ or } 0 \text{ V}.$$  

With $V_G = 0$ and $V_{GS} = 4$ V then $V_S = -4$ V. Hence,

$$R_S = \frac{-4 - (-10)}{1 \text{ mA}} = 6 \text{ k}\Omega$$

Lastly, for a 1-M\Omega AC input resistance, then referring to the input portion of the small-signal model
we see that

\[ R_{in} = R_G \Rightarrow R_G = 1 \, \text{M}\Omega \]

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**Biasing IC MOSFET Amplifiers. Current Mirrors.**

For MOSFET amplifier biasing in ICs, **DC current sources** are usually used. As discussed in Lecture 17, “golden currents” are produced using sophisticated multi-component circuits. Then current mirroring (aka current steering) circuits are used to replicate this golden current to provide DC biasing currents at different points in the IC.

The basic MOSFET **current mirror** is shown in Fig. 4.33b for **NMOS**. (This is basically the same circuit we saw with the BJT current mirror in Lecture 17.)
$Q_1$ has the drain and gate terminals connected together. This forces $Q_1$ to operate in the saturation mode in this particular circuit if $I_{D1} \neq 0$. In this mode,

$$I_{D1} = \frac{1}{2} k_{n1}' \frac{W_1}{L_1} (V_{GS} - V_{t1})^2$$  \hspace{1cm} (4.50) \hspace{0.5cm} (1)$$

With a zero gate current,

$$I_{REF} = I_{D1}$$  \hspace{1cm} (2)$$

where we can easily see from the above circuit that

$$I_{REF} = \frac{V_{DD} - V_{GS} - (-V_{SS})}{R}$$  \hspace{1cm} (4.51) \hspace{0.5cm} (3)$$

Now, we’ll assume the two MOSFETs in the circuit have the same $V_{GS}$. Consequently, the drain current in the second transistor is

$$I_{D2} = \frac{1}{2} k_{n2}' \frac{W_2}{L_2} (V_{GS} - V_{t2})^2$$  \hspace{1cm} (4)$$
If these two transistors are perfectly matched but perhaps fabricated with different channel dimensions, then $k_{n1}' = k_{n2}'$, and $V_{t1} = V_{t2}$ so that we see by comparing (1) and (4) that

$$I_{D2} = \frac{W_2/L_2}{W_1/L_1} I_{D1} = \frac{W_2/L_2}{W_1/L_1} I_{REF} \quad (4.53),(5)$$

In this NMOS current mirror shown above, $Q_2$ acts as a current sink since it pulls current $I_O = I_{D2}$ from the load, which is the amplifier circuit of Fig. 4.33a in this case.

In PMOS this current mirror circuit is constructed as

Here $Q_2$ acts as a current source since it pushes current $I_O = I_{D2}$ into the load.

**Example N30.2.** Design an NMOS current mirror with $V_{DD} = 5$ V, $V_{SS} = 0$, and $I_{REF} = 100$ μA. For the matched transistors $L = 10$ μm, $W = 100$ μm, $V_t = 1$ V, and $k_n' = 20$ μA/V^2.
Referring to the NMOS current mirror circuit in Fig. 4.33b above, notice that the drain of $Q_1$ is connected to its gate so that $V_{GD1} = 0$, which is less than $V_t$. This means $Q_1$ is operating in the \textbf{saturation mode} (or is possibly cutoff).

Assuming operation in saturation,

$$I_{D1} = I_{REF} = \frac{1}{2} k'_n \frac{W}{L} (V_{GS} - V_t)^2$$

$$= \frac{1}{2} \cdot 20 \times 10^{-6} \cdot \frac{100}{10} \cdot (V_{GS} - 1)^2$$

For $I_{REF} = 100 \, \mu A$ $\Rightarrow$ $100 = 10 \cdot 10 (V_{GS} - 1)^2$ or

$$V_{GS} = \pm 1 + 1 = 2 \, \text{V or 0 V}$$

Now, by KVL

$$V_{DD} = I_{REF} R + V_{GS}$$

With $V_{GS} = 2 \, \text{V}$ then

$$R = \frac{V_{DD} - V_{GS}}{I_{REF}} = \frac{5 - 2}{100 \, \mu A} = 30 \, \text{k\Omega}$$

Here are a few additional questions based on this design:

- What is the lowest possible value for $V_O = V_{D2}$ and still have a functioning current mirror?

As with $Q_1$, the transistor $Q_2$ must also operate in \textbf{saturation} if it’s going to supply a constant current.
Hence
\[ V_{GD2} \leq V_t \Rightarrow V_{G2} - V_{D2} \leq V_t \]
\[ \therefore V_O = V_{D2} \geq V_{G2} - V_t \]
or
\[ V_O \geq V_{GS} - V_t = 2 - 1 = 1 \text{ V} \]

Therefore,
\[ V_O \big|_{\text{min}} = 1 \text{ V} \]

- Imagine that \( V_A = 10^7 L \). (Notice that \( V_A \) is proportional to the channel length, which is commonplace.) What is \( r_o \)?

\[ V_A = 10^7 \cdot 10 \times 10^{-6} = 100 \text{ V} \]

\[ r_o = \frac{V_A}{I_O} = \frac{100}{100 \mu A} = 1 \text{ M\Omega} \]

- What is change in the output current \( I_O \) if \( V_O \) changes by 3 V?

\[ \Delta I_O = \frac{\Delta V_O}{r_o} = \frac{3 \text{ V}}{1 \text{ M\Omega}} = 3 \mu A \]