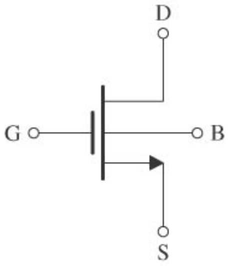
Lecture 26: MOSFET Circuit Symbols, i_D-v_{DS} Characteristics.

There are two circuit symbols you may encounter for the enhancement type MOSFET. For the *n*-channel, one symbol is



(Fig. 5.11b)

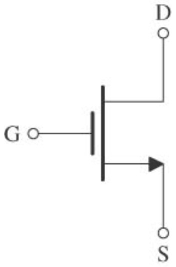
Referring to this circuit symbol:

✓ The arrowed terminal indicates the source,

✓ This arrow direction indicates *n*-type (direction of current)

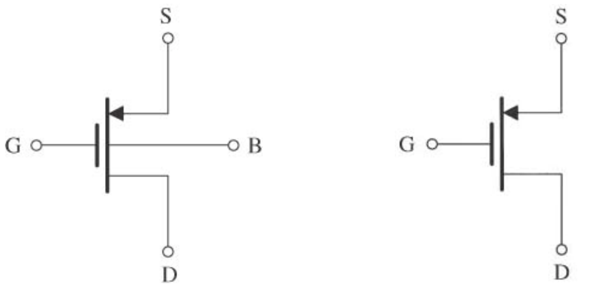
✓ The gap at the gate indicates the oxide layer.

However, the body is often connected to the source. This leads to a more common circuit symbol:



(Fig. 5.11c)

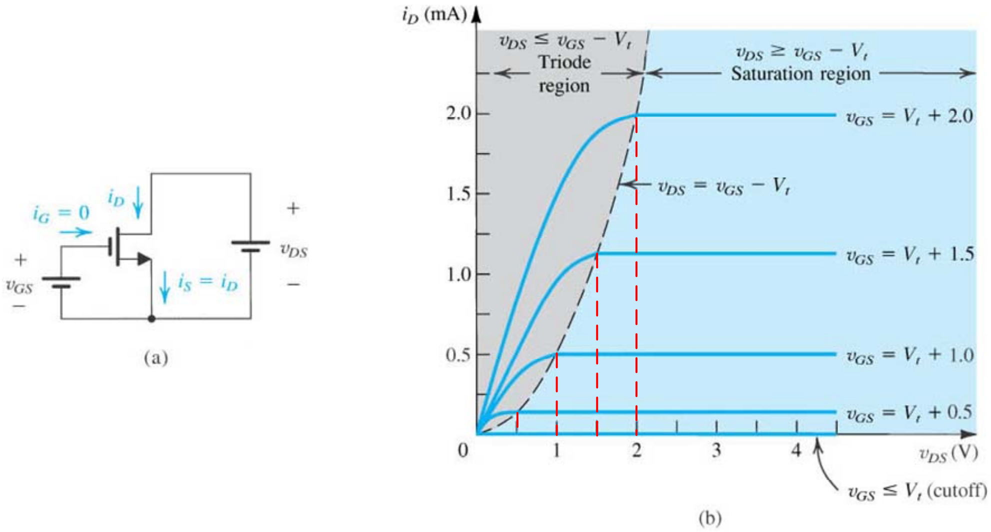
Similar circuit symbols are used for *p*-channel enhancement type MOSFETS:



(Figs. 5.19b,c)

MOSFET i_D–v_{DS} **Characteristics**

Similar to a BJT, we can generate a set of i_D–v_{DS} characteristic curves for a MOSFET by setting v_{GS} and varying v_{DS}. This is shown in Fig. 1 (or, similarly, Fig. 5.13) for an *n*-type MOSFET:



(Fig. 1)

(Sedra and Smith, 5th ed.)

There are three regions of operation:

(1) **Cutoff**. To operate an enhancement type MOSFET, we first must induce the channel. For NMOS, this means that

$$v_{GS} \geq V_t \quad \text{(induce)} \tag{1}$$

If $v_{GS} < V_t$ there is no channel and the device is cutoff, which we see in Fig. 1.

When the MOSFET is cutoff, $i_D = i_S = 0$.

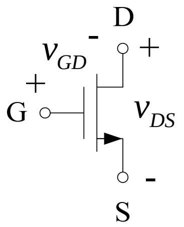
(2) **Triode**. To operate in this mode, we first must induce the channel as in (1) above.

We must also keep v_{DS} small enough so the channel is continuous (not pinched off):

$$\boxed{v_{GD} > V_t \quad \text{(continuous)}} \tag{2}$$

[Note how similar this last criterion is to $v_{GS} > V_t$ for the channel to be induced. Here in (2), we have $v_{GD} > V_t$ for a continuous channel at the drain end. This observation can help us to remember these criterion.]

Another way of writing this criterion in (2) is in terms of v_{DS}. Referring to this circuit element



we see that

$$v_{DS} = v_{GS} + v_{DG} \tag{3}$$

For a continuous channel, as required by (2), (3) becomes

$$v_{DS} - v_{GS} = v_{DG} < -V_t$$

Therefore,

$$\boxed{v_{DS} < v_{GS} - V_t \quad \text{(continuous)}} \tag{4}$$

We can use either (2) or (4) to check for triode operation of the MOSFET.

As given in the last lecture, in the triode region

$$i_D = k_n' \frac{W}{L}\left[\left(v_{GS} - V_t\right)v_{DS} - \frac{1}{2}v_{DS}^2\right] \qquad (5.16),(5)$$

If $v_{DS}^2/2 \ll \left(v_{GS} - V_t\right)v_{DS}$ then

$$i_D \approx \underbrace{k_n' \frac{W}{L}\left(v_{GS} - V_t\right)}_{g_{DS} \equiv r_{DS}^{-1}} v_{DS} \equiv g_{DS} v_{DS} \qquad (5.10),(6)$$

where $r_{DS} \equiv g_{DS}^{-1}$ is defined as the (linear) resistance between the drain and source terminals. The value of r_{DS} is controlled by v_{GS}. (See Fig. 5.4).

(3) **Saturation**. To operate in this mode we need to first induce the channel

$$v_{GS} \geq V_t \quad \text{(induce)} \tag{7}$$

then ensure that the channel is pinched off at the drain end

$$\boxed{v_{GD} \leq V_t \quad \text{(pinch off)}} \tag{8}$$

or equivalently

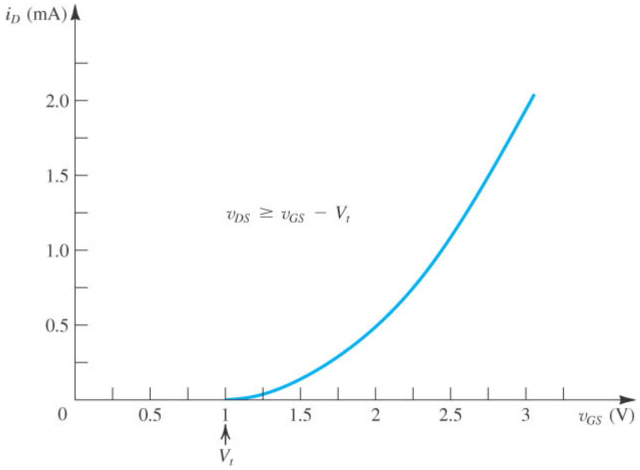
$$\boxed{v_{DS} \geq v_{GS} - V_t \quad \text{(pinch off)}} \tag{9}$$

As we saw in the previous lecture, the drain current in this region is

$$i_D = \frac{1}{2} k_n' \frac{W}{L} \left(v_{GS} - V_t \right)^2 \qquad (5.20),(10)$$

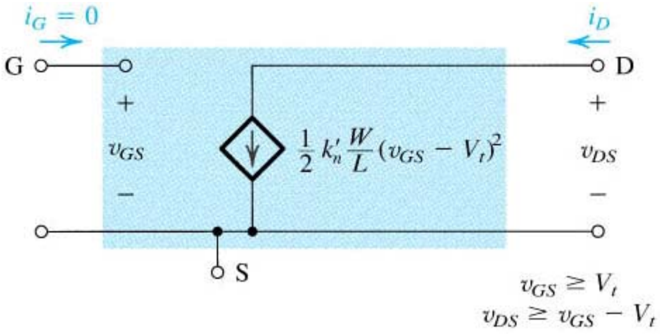
and is not dependent on v_{DS}, as shown in Fig. 1.

A plot of i_D versus v_{GS} for an enhancement type NMOS device in saturation is shown in Fig. 5.14:



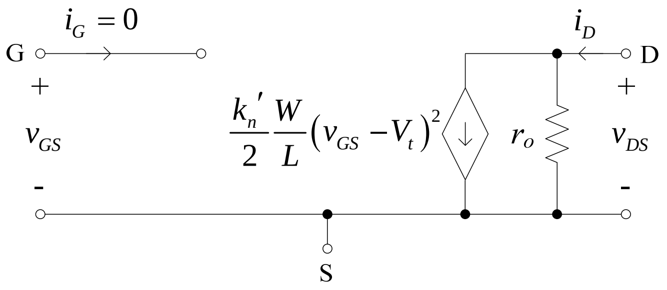
(Fig. 5.14)

In the saturation mode, this device behaves as an ideal current source controlled by v_{GS}:



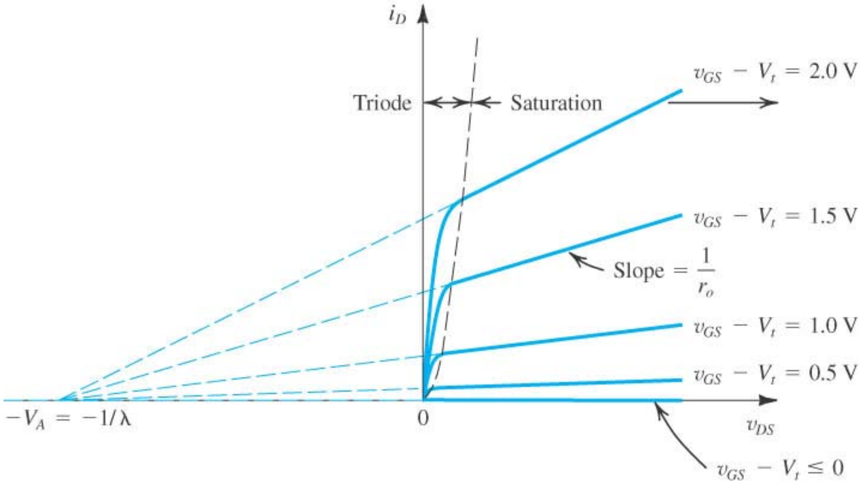
(Fig. 5.15)

In reality, though, there is a finite output resistance (r_o) that should be added to this model:



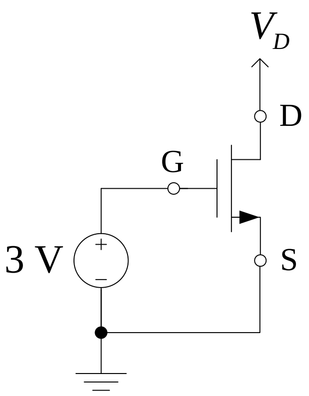
where $$r_o = \frac{V_A}{I_D'} \qquad (5.27),(11)$$

This finite output resistance gives a slope to the i_D–v_{DS} characteristic curves:



(Fig. 5.17)

Example N26.1 Given an enhancement type NMOS with $V_t = 2$ V.



Determine the region of operation of this device for the following V_D. Use these criteria for the region of operation:

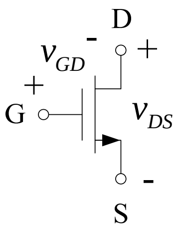
- Cutoff: $v_{GS} < V_t$
- Triode: $v_{GS} \geq V_t$ and $v_{DS} < v_{GS} - V_t$
- Saturation: $v_{GS} \geq V_t$ and $v_{DS} \geq v_{GS} - V_t$

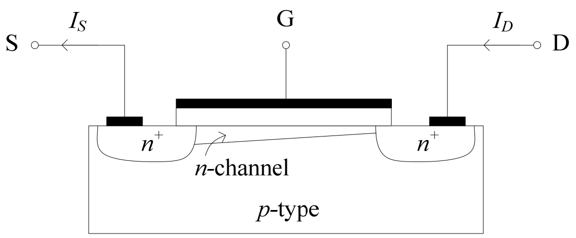
(a) $\underline{V_D = 0.5\text{ V}}$. $V_{GS} = 3\text{ V} > V_t = 2\text{ V} \Rightarrow$ not cutoff. Then $V_{DS} = 0.5\text{ V} < V_{GS} - V_t\ (= 3 - 2 = 1\text{ V})$. $\therefore$ triode mode.

(b) $\underline{V_D = 1\text{ V}}$. $V_{GS} = 3\text{ V} > V_t = 2\text{ V} \Rightarrow$ not cutoff. Then $V_{DS} = 1\text{ V} = V_{GS} - V_t$ (= 1 V). $\therefore$ saturation (or triode) mode.

(c) $\underline{V_D = 5\text{ V}}$. $V_{GS} = 3\text{ V} > V_t = 2\text{ V} \Rightarrow$ not cutoff. Then $V_{DS} = 5\text{ V} > V_{GS} - V_t$ (= 1 V). $\therefore$ saturation mode.

Example N26.2 (similar to text Problem 5.22). An NMOS enhancement type MOSFET has $V_t = 2$ V. If V_{GS} ranges from 2.5 to 5 V what is the largest V_{DS} for which the channel remains continuous?





✓ $V_{GS} > V_t$, $\forall V_{GS}$ so the channel is always present.

✓ Then for the channel to remain open at the drain end,

$$V_{DS} < V_{GS} - V_t \quad \text{(triode)}$$

Which V_{GS} to use here? The smallest. Therefore,

$$V_{DS}\big|_{\max} < 2.5 - 2 = 0.5 \text{ V}$$