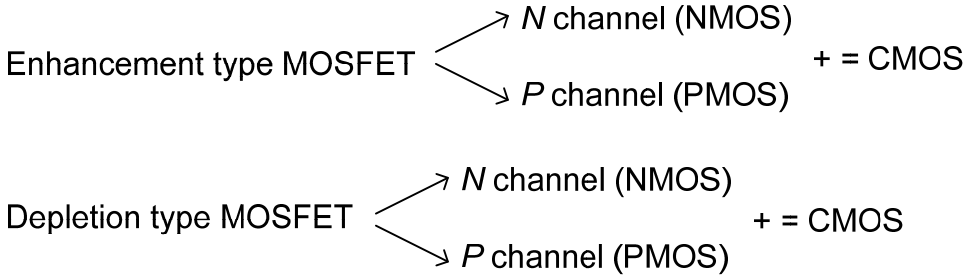
Lecture 25: Enhancement Type MOSFET Operation, *P*-channel, and CMOS.

We will now move on to the second major type of transistor called the field effect transistor (FET). In particular, we will examine in detail the metal oxide semiconductor FET (MOSFET). This is an extremely popular type of transistor.

MOSFETs have similar uses as BJTs. They can be used as signal amplifiers and electronic switches, for example. MOSFETS can be manufactured using a relatively simple process and made very small with respect to BJTs.

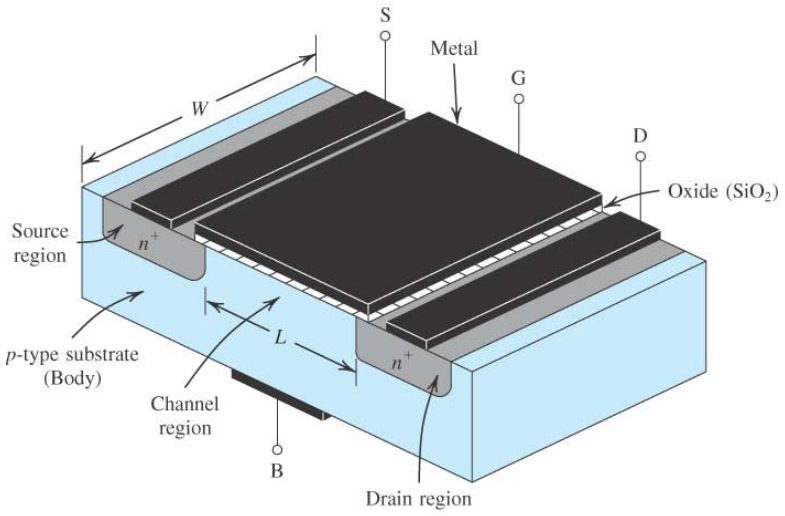
There are two major types of MOSFETS, called enhancement type and depletion type. Each of these types can be manufactured with a so-called *n* channel or *p* channel:



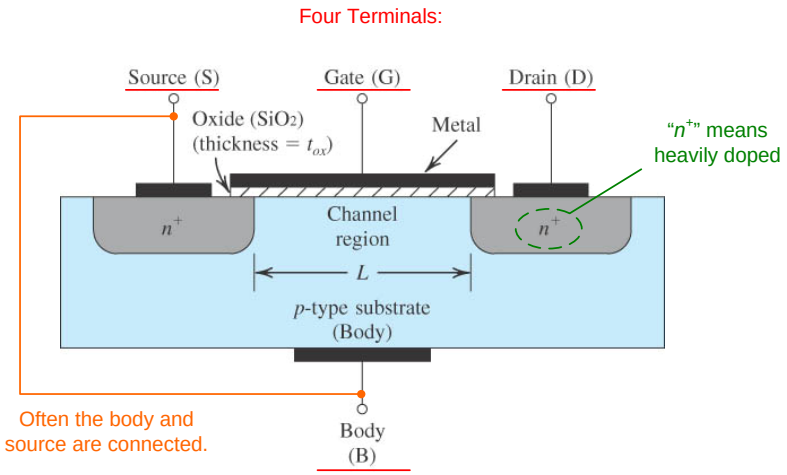
Enhancement Type, *N* Channel MOSFET

The enhancement type MOSFET is the most widely used FET. It finds extensive use in VLSI circuits, for example. (In general, MOSFETs are not used too often in discrete component design.)

The physical structure of this type of MOSFET (enhancement type NMOS) is shown in Fig. 5.1:



(Fig. 5.1a)



(Fig. 5.1b)

Typical dimensional values are L = 0.1 to 3 μm, W = 0.2 to 100 μm, and t_{ox} = 2 to 50 nm.

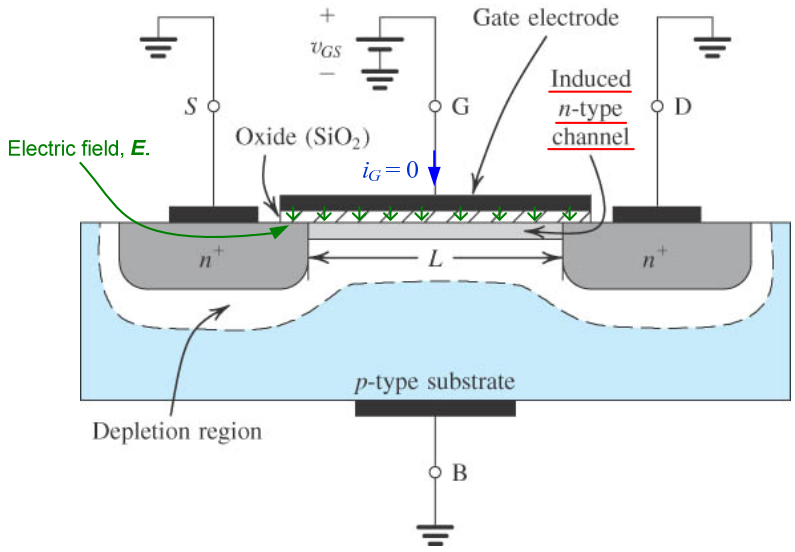
The minimum L and W dimensions are dictated by the resolution of the lithography process used to create the device. Around the 2007 time frame, Intel developed a 45-nm process, as described in the attached article from IEEE *Spectrum*. To avoid the so-called "short channel" effects, the channel length is made generally two to five times larger than the smallest possible feature sizes. Consequently, one could expect the channel length to be ~90 nm to 225 nm for the MOSFETs fabricated by this process.

More recently, Samsung has developed a 10-nm process allow for even greater miniaturization of integrated circuits.

Notice in the figures on the previous page that the MOSFET device has four terminals, though often the body and source terminals are connected together forming a three terminal device.

With no bias voltage applied to the gate terminal, there exists two back-to-back *pn* junctions between the drain and the source. No current flows from drain to source (the resistance will be on the order of 10^{12} Ω).

In order to obtain current flow the MOSFET needs to be biased, similar to what is required for BJTs. For the MOSFET, however, we apply a voltage to the gate with respect to the source: v_{GS}. Because of the oxide layer under the gate electrode, the gate current will be essentially zero.



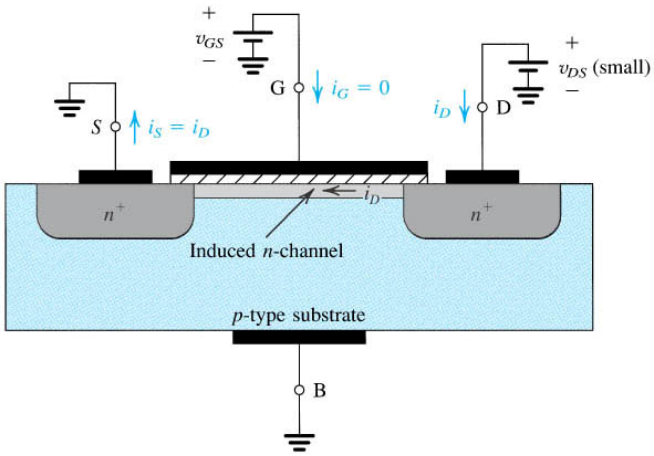
(Fig. 5.2)

In effect, the gate and the channel region form a parallel plate capacitor of sorts around the oxide layer. Two things happen when v_{GS} is applied:

1. Free holes in the *p*-type substrate are repelled from the region under the gate. This process "uncovers" bound negative charge.
2. Electrons from the heavily doped n^+ regions (the drain and source) are attracted under the gate.

These effects create an induced *n*-type **channel**. Notice that this bias voltage v_{GS} is required in order to create the channel: no v_{GS}, no channel. This is called "inducing" the channel.

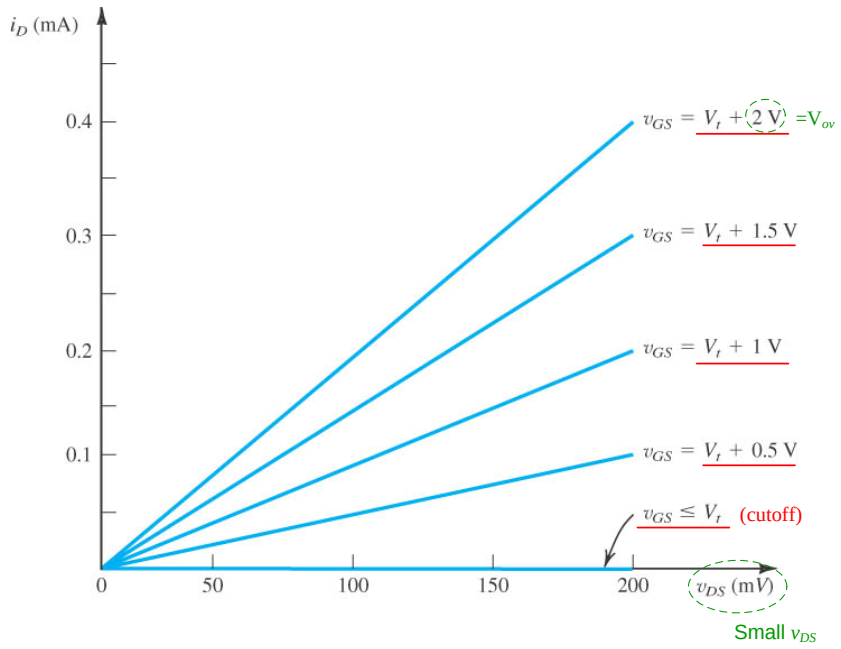
Now, if a voltage is applied between the drain and source, as in Fig. 5.3, we will have a flow of electrons from source to drain (i.e., a current). This is the origin of the names "source" and "drain."



(Fig. 5.3)

The v_{GS} required to accumulate sufficient numbers of mobile electrons in the channel is called the threshold voltage V_t. For an n-channel MOSFET, $V_t \approx 1-3$ V (note that this is a positive voltage).

A family of i_D-v_{DS} characteristic curves for the MOSFET with a small v_{DS} is shown in Fig. 5.4 with v_{GS} as the parameter:



(Fig. 5.4)

In this mode, the transistor is behaving like a resistor between the drain and source terminals whose resistance is controlled by v_{GS}.

It is apparent from the varying slopes of these lines in Fig. 5.4 that the conductance of this channel is proportional to the so-called excess gate voltage or overdrive voltage

$$V_{OV} \equiv v_{GS} - V_t \qquad (5.1),(1)$$

which must be greater than zero for current to exist from drain to source.

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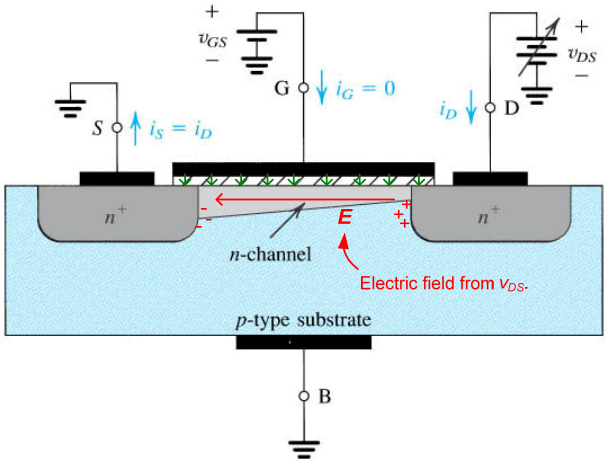
i_D-v_{DS} for Larger v_{DS}

The behavior of the MOSFET changes considerably when v_{DS} increases beyond small values:



(Fig. 5.5)

In these circumstances, an additional electric field is created from drain to source that is large enough to alter the shape of the channel. With the partial electric field due to v_{DS} directed as shown above, there exists more negative charges near the source end of the channel than at the drain end. This produces a thicker channel near the source than the drain.

Alternatively, it is the gate voltage relative to points along the channel that gives rise to the thickness of the channel. At the source end using (1)

$$v_G - v_S = v_{GS} = V_{OV} + V_t$$

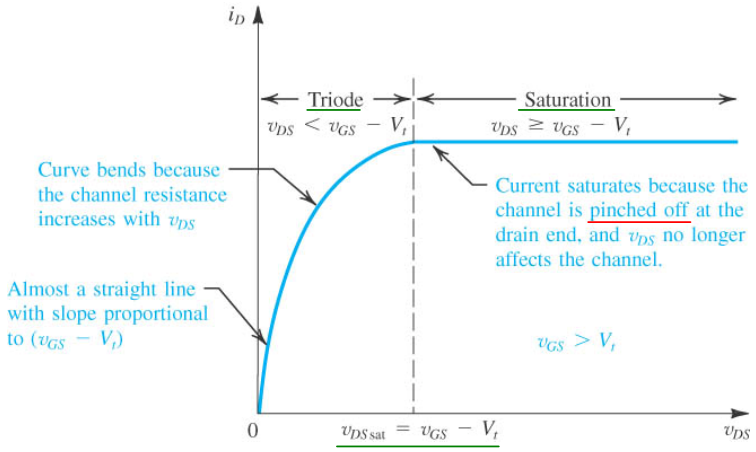
while at the drain end

$$v_{GD} = v_{GS} - v_{DS} \underbrace{=}_{(1)} V_{OV} + V_t - v_{DS}$$

These voltages at the two extremes of the gate indicate the voltage is getting smaller as we move from the source end of the gate towards the drain end of the gate. Consequently, we would expect the channel depth to change as well.

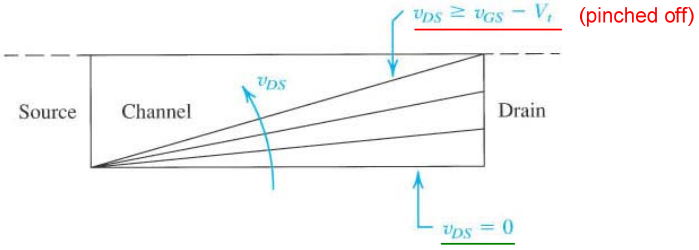
Because of this tapered shape of the channel, the resistance of the channel increases relative to that with a uniform depth.

Hence, the i_D-v_{DS} characteristic curve is no longer a straight line:



(Fig. 5.7)

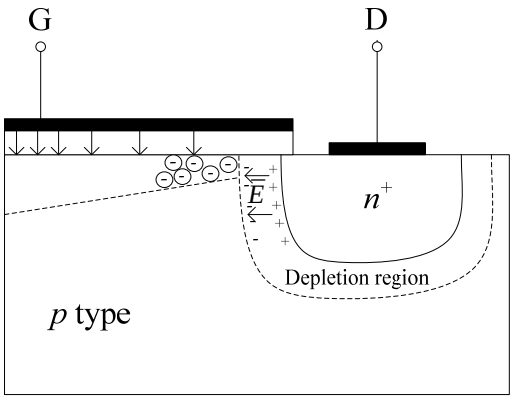
Note that it is possible to increase v_{DS} large enough to reduce the channel thickness to zero at the drain end.



(Fig. 1)
(Sedra and Smith, 5th ed.)

This is called **pinch off** ($v_{DS} \geq v_{GS} - V_t$).

Does this mean that the current $i_D = 0$? Actually, it does not. A MOSFET that is "pinched off" at the drain end of the channel still conducts current:



The large $\bar{E}$ in the depletion region surrounding the drain will sweep electrons across the end of the pinched off channel to the drain (See Lecture 2).

This is very similar to the operation of the BJT. For an *npn* BJT, the electric field of the reversed biased CBJ swept electrons from the base to the collector regions.

Regions of MOSFET Operation

There are three regions of operation for a MOSFET:

1. Off or cutoff region, where $i_D = 0$.
2. "Triode" region, where

$$v_{DS} < v_{DS}\big|_{\text{sat}} = v_{GS} - V_t \qquad (5.18),(1)$$

3. "Saturation" region, where

$$v_{DS} > v_{DS}\big|_{\text{sat}} \qquad (2)$$

The term saturation has a very different meaning for MOSFETs than for BJTs.

As derived in the text, the i_D-v_{GS} relationships for MOSFETs are given mathematically as

- Triode region: $$i_D = k_n' \frac{W}{L}\left[\left(v_{GS} - V_t\right)v_{DS} - \frac{v_{DS}^2}{2}\right] \qquad (5.14),(3)$$

- Saturation region: $$i_D = \frac{1}{2}k_n' \frac{W}{L}\left(v_{GS} - V_t\right)^2 \qquad (5.17),(4)$$

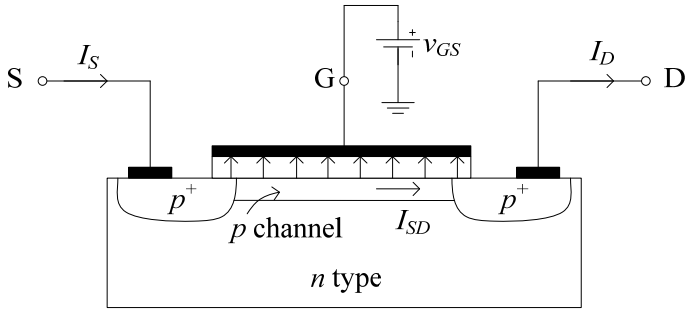
where k_n' is the process transconductance parameter [A/V^2] and is equal to

$$k_n' = \mu_n C_{ox} = \mu_n \frac{\varepsilon_{ox}}{t_{ox}} \qquad (5.11),(5)$$

Here, μ_n is the mobility of electrons in the channel [cm^2/(V-s)], C_{ox} is the capacitance per unit gate area [F/m^2], and ε_{ox} and t_{ox} are the permittivity and thickness of the gate oxide layer, respectively.

Enhancement-Type *P*-Channel MOSFET

The *p*-channel MOSFET (PMOS) is manufactured similarly to the NMOS:

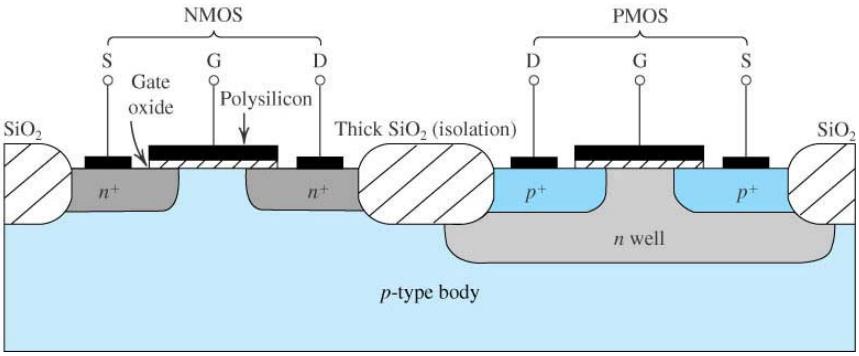


Holes are the charge carriers in the *p*-type channel. When operating this device: $v_{GS} < 0$, $v_{DS} < 0$, and $V_{tp} < 0$.

PMOS was originally the dominant MOSFET, but was replaced by NMOS. NMOS can be manufactured smaller than PMOS and operate faster.

Complementary MOS (CMOS)

CMOS are transistor circuits formed from a combination of NMOS and PMOS devices in the same circuit. Very popular.



(Fig. 5.10)